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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,181	12/02/2003	Richard Thomas Plunkett	PEA01US	6713

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EXAMINER	
KAU, STEVEN Y	

ART UNIT	PAPER NUMBER
2625	

NOTIFICATION DATE	DELIVERY MODE
01/15/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/727,181	PLUNKETT ET AL.	
	Examiner	Art Unit	
	STEVEN KAU	2625	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 07 January 2010 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-6*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.

12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____.

/David K Moore/
Supervisory Patent Examiner, Art Unit 2625

/Steven Kau/
Examiner, Art Unit 2625

Continuation of 11. does NOT place the application in condition for allowance because: Applicants' Remarks/Arguments with respect to claim 1 rejection under 35 U.S.C. 103(a) have been fully considered and are not persuasive.

MPEP 2111: During patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification" Applicant always has the opportunity to amend the claims during prosecution and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 162 USPQ 541,550-51 (CCPA 1969). The court found that applicant was advocating ... the impermissible importation of subject matter from the specification into the claim. See also In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997) (The court held that the PTO is not required, in the course of prosecution, to interpret claims in applications in the same manner as a court would interpret claims in an infringement suit. Rather, the "PTO applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definition or otherwise that may be afforded by the written description contained in application's specification."). The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. In re Cortright, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999).

MPEP 2141.02: In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); Schenck v. Nortron Corp., 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983) (Claims were directed to a vibratory testing machine (a hard-bearing wheel balancer) comprising a holding structure, a base structure, and a supporting means which form "a single integral and gaplessly continuous piece." Nortron argued the invention is just making integral what had been made in four bolted pieces, improperly limiting the focus to a structural difference from the prior art and failing to consider the invention as a whole. The prior art perceived a need for mechanisms to dampen resonance, whereas the inventor eliminated the need for dampening via the one-piece gapless support structure. "Because that insight was contrary to the understandings and expectations of the art, the structure effectuating it would not have been obvious to those skilled in the art." 713 F.2d at 785, 218 USPQ at 700 (citations omitted).). See also In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) (Claims were directed to a three step process for preparing sweetened foods and drinks. The first two steps were directed to a process of producing high purity maltose (the sweetener), and the third was directed to adding the maltose to foods and drinks. The parties agreed that the first two steps were unobvious but formed a known product and the third step was obvious. The Solicitor argued the preamble was directed to a process for preparing foods and drinks sweetened mildly and thus the specific method of making the high purity maltose (the first two steps in the claimed process) should not be given weight, analogizing with product-by-process claims. The court held "due to the admitted unobviousness of the first two steps of the claimed combination of steps, the subject matter as a whole would not have been obvious to one of ordinary skill in the art at the time the invention was made." 535 F.2d at 69, 190 USPQ at 17 (emphasis in original). The preamble only recited the purpose of the process and did not limit the body of the claim. Therefore, the claimed process was a three step process, not the product formed by two steps of the process or the third step of using that product.).

MPEP 2106: Limitations appearing in the specification but not recited in the claim should not be read into the claim. E-Pass Techs., Inc. v. 3Com Corp., 343 F.3d 1364, 1369, 67 USPQ2d 1947, 1950 (Fed. Cir. 2003) (claims must be interpreted "in view of the specification" without importing limitations from the specification into the claims unnecessarily). In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also In re Zletz, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow.... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed.... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process.").

With respect to arguments, pages 2-3, that the combination of prior arts of Shu (US 5,594,839), Schmidt (US 5,193,012) and Hashmoto (US 4,999,814) do not teach the feature of "steps (a) to (c) are performed simultaneously with step (d)".

Applicants argued, "Col. 1, lines 61 - 66
This portion of Hashimoto describes that sense amplifiers are provided with the write line buffer and read line buffer for parallel input and output, respectively. In this context, that parallel input and parallel output do not mean that input and output are performed simultaneously. " "Rather, "parallel input" means that data is inputted in parallel as opposed to serially. Similarly, "parallel output" means that data is outputted in parallel as opposed to serially. Indeed, this is illustrated in Fig. 1, where each row and column line of the DRAM has its own connection to the write line buffer and the read line buffer."

"That Examiner has mistakenly understood the description of '...parallel input and output, respectively.' to mean that input and output are performed simultaneously.

"In fact, this portion of Hashimoto does not teach or suggest simultaneous input and output of data from a buffer. The use of the word "respectively" in this description of Hashimoto supports Applicant's position that Applicant's interpretation of Hashimoto is the correct technical interpretation."

In re, the Examiner respectfully disagrees with the arguments. The relationship of "parallel input" and "parallel output" is clearly disclosed in the paragraph, recites, "In FIG. 1, for sake of descriptional convenience, it is assumed that 200 parallel sense amplifiers are provided in the direction of row of dynamic memory elements with the write line buffer and read line buffer connected to these sense amplifiers for

parallel input and output, respectively. There is continuous input of serial data to the write line buffer with serial data read out from the read line buffer for continuous output. For both of these input and output circuits, any known means for serial data input or output with an exclusive addressing circuit built in may be used. Such input and output circuits can also be materialized otherwise by an approach as applied to the VRAM (Video RAM), etc. Accordingly, the operation of line buffers is omitted from the following description of this specification." Based on this teaching, the Examiner disagrees, that "Rather, "parallel input" means that data is inputted in parallel as opposed to serially. Similarly, "parallel output" means that data is outputted in parallel as opposed to serially. Indeed, this is illustrated in Fig. 1, where each row and column line of the DRAM has its own connection to the write line buffer and the read line buffer." The above disclosure is clearly teaching that "There is continuous input of serial data to the write line buffer with serial data read out from the read line buffer for continuous output" , and it is clearly that there is no such meaning for ""parallel input" means that data is inputted in parallel as opposed to serially. Similarly, "parallel output" means that data is outputted in parallel as opposed to serially." Rather, it teaches input and output are performed in parallel, or simultaneously.

Applicants argued, that "Col. 6, lines 31 - 40
Applicant firstly notes that this portion of Hashimoto is part of claim 5. Accordingly, Applicant respectfully submits that this description alone is not enabling, and accordingly does not teach or suggest the feature at issue. The claims of a patent should be supported by their description, and accordingly, the description that supports this feature of claim 5 of Hashimoto should be referred to instead of claim 5 itself."

In re, the Examiner respectfully disagrees with the assertion. With respect to Claim 5, limitations recite, "A method according to claim 2, wherein, in repeated step (b), it is determined whether dither values at an end position in the memory have been read for each of the dither matrices, and if so, the updated start position is updated to the initial start position." The Examiner refers the Applicants to the final Action, pages 13-16, 11/21/2009, where limitations are taught by Shu in view of Schmidt and Hashimoto and further in view of Yamashita.

Applicants further argued, "Even if, for the sake or argument, one were to assume that Hashimoto did teach simultaneously reading writing into/from the write line and read line buffers, such an operation concerns two separate buffers and does not relate to one buffer memory. Claim 1 concerns outputting dither values into and from the same buffer memory. Accordingly, teaching concerning outputting data from a first buffer simultaneously with inputting data to a second different buffer does not prejudice this feature of claim 1."

In re, the Examiner again respectfully disagrees with the arguments. With respect to Claim 1, limitations recite, "A method for sequentially outputting full lines of dither values of a dither matrix stored in a memory, comprising the steps of:
(a) reading a plurality of dither values of the dither matrix from the memory into a buffer memory, the reading commencing at a start position in the memory until a full line of dither values of the dither matrix has been read;
(b) updating the start position to an updated start position in the memory of a subsequent line of dither values;
(c) outputting the full line of dither values into the buffer memory;
(d) outputting a full line of dither values from the buffer memory, said outputting of dither values from the buffer memory commencing after a full line of dither values has been output into the buffer memory;
(e) repeating steps (a) - (c) until all lines of dither values of the dither matrix have been read and output to the buffer memory, wherein after a first iteration of steps (a) - (c), steps (a) to (c) are performed simultaneously with step (d)." (emphasis added by the examiner). The claim language is clearly stated for multiple memories, i.e. "the memory" and "a buffer memory". Thus, the argument of "Claim 1 concerns outputting dither values into and from the same buffer memory" is not persuasive.

As explained in detail in the previous Action, a prima facie obviousness has been established and clearly explained in the previous Action.

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

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01/11/2009 .